Development of the CMS Pixel detector

W. Erdmann[a]

[a]ETH-Zürich, Institute for Particle Physics, CH 5232 Villigen PSI, Switzerland

A readout chip for the CMS Pixel detector has been developed in the radiation hard DMILL process. The chips ability to operate under LHC conditions was tested in a high rate pion beam with track densities up to 3×10^7 cm^{-2}s^{-1}. The observed degradation of the detection efficiency with increasing particle flux is compared with the data-loss mechanisms inherent to the readout architecture. First detector modules with 16 chips on a low mass high density interconnect are being evaluated. The next iteration of the readout chip is designed for a 0.25 μm process with radiation tolerant layout.

1. The CMS pixel detector

A pixel detector will be the innermost tracking device of the CMS experiment at the Large Hadron Collider (LHC). It provides high resolution track measurements close the the interaction point for precise vertex determination and fine granularity that is essential for pattern recognition in this region of highest track density.

Silicon sensors with n-side readout will be used to allow operation even beyond the point where full depletion is no longer possible due to radiation damage. A maximum bias voltage of 500 V is foreseen. The Lorentz drift of the electrons inside the strong magnetic field of 4 T leads to charge spreading at the readout side of the order of 150 μm for an un-irradiated sensor of 300 μm thickness. With pixels of similar size the charge will be collected in more than one pixel. Interpolation based on the amount of charge can give good spatial resolution for a moderate pulse-height accuracy corresponding to 3-4 bits and front-end thresholds of 2000-3000 electrons [2]. The readout of the CMS pixel detector is fully analog.

The original design foresees 150 μm wide pixels in the drift direction for which space requirements of the readout circuitry per pixel allow the same size in the other direction. Charge sharing in the disks is a achieved by tilting the segments so that the drift direction is not parallel to the magnetic field. The reduction in depletion depth or the increase in bias voltage will lead to a reduction of charge sharing and therefore a degradation of the spatial resolution with radiation damage. The final detector will have a pixel size of 100 μm to maintain a good resolution up to higher doses of irradiation.

The detector has a barrel geometry with layers at 4 cm, 7 cm and 11 cm in the central region, ±26 cm around the interaction point, while disks cover the high rapidity region. Readout chips are bump-bonded to the sensors with indium bumps. With 3×10^6 channels and 5×10^3 hits per bunch crossing in the barrel region, only zero-suppressed data for events selected by the CMS trigger can be read-out. The readout chip must detect sensor signals above a threshold, assign them to the correct bunch crossing, which occur at 25 ns intervals, and store the hit information during the 3.2 μs latency of the CMS trigger. Only a small fraction of the events are read out and the chip must remain sensitive for new hits while waiting for a trigger decision. A column drain architecture [2] was chosen for the CMS pixel readout chip, where pixels send hit data to buffers outside the active region as soon as possible and then resume data-taking. This architecture permits a relatively simple pixel cell design, but creates a large data-flow inside the readout chip and high rates with stochastic fluctuations can lead to dead-times and data-losses. These must be assessed with detailed simulations and were measured for the first time in a high rate test beam.

2. The DMILL readout chip

A readout chip for the CMS pixel detector has been developed using the radiation hard DMILL technology [3]. The first full-size chip, PSI43, was fabricated in 2002. It is fully functional and the production yield was 20%.

The active region of PSI43 has a size of 8 mm $\times$ 8 mm and consists of 52×53 quadratic pixel cells with a size of 150 μm. The pixels are organized into 26 double columns of 2×53 pixels. As hits arrive, the information flows down vertical buses to the data- and time-stamp buffers in the periphery of the double-columns. Double columns operate independently of each other unless they contain data verified by a trigger and wait for a readout.

Data losses occur at several stages in the readout chain when the local buffering capability is exceeded [4]. The buffering requirements are determined by the rate of incoming data and the amount time until the buffer is free again because the data can be passed on or discarded. The pixel cell itself can only store a single hit, the buffers in each column periphery hold 24 hits from up to 9 events. The size of these buffers dominates the length of the chip periphery and is constrained by the detector layout. The collection of hit-data belonging to the same bunch crossing happens in token scans inside a double column. The token scan is initiated when any of the pixels signals a hit over a wired OR. New hits can be handled during an on-going column drain, however with two limitations: Only one pending column drain is stored hits and cannot arrive in two consecutive bunch crossings. No event buffer exists so that dead time also occurs during read-out, but only in double-columns with hits from triggered events.

Simulations based on the expected particle fluences in CMS showed that this architecture results in data-losses of the order of 2% or less for the foreseen scenarios, i.e. the 4 cm and 7 cm layers with low luminosity LHC operation or the 7 cm and 11 cm layers for high luminosity LHC operation.

A single chip assembly was operated in a high rate test beam at PSI to verify that the chip can operate under LHC conditions. The intensity of the 300 MeV/c pion beam was adjustable up to 3×10^7 cm^{-2}s^{-1}, which is more than expected in the 4 cm layer at full LHC luminosity. A telescope made of 2 mm $\times$ 2 mm $\times$ 2 mm scintillators monitored the beam intensity and provided a beam trigger for particles hitting the assembly.

The PSI accelerator has a beam structure of 50 MHz while the chip was operated with a synchronized 40 MHz clock. Every fifth pion bunch had the correct timing relative to the chip clock and triggers were only issued for such events. The scintillator trigger rate was scaled down by requiring a coincidence with a random signal from a radioactive source in order to model the CMS trigger.

The beam spot was large enough to cover the full chip and randomly triggered events show a uniform distribution of hits. The observed hit pattern in events triggered with the beam telescope reflects the shape and size of the scintillators.

The readout architecture can be tested by injecting artificial hits using the calibration mechanism. As expected those hits are read out with 100% efficiency when no beam is present. With increasing beam intensity the rate of missing hits grows almost linearly reaching 2% at 3×10^7 cm^{-2}s^{-1}, in agreement with simulations of the test beam operation. Because all tracks are perpendicular to the sensor and the absence of a magnetic field, the pixel multiplicity per track was close to one and the relative importance of the various data-loss mechanisms is different from CMS operation. The largest contribution in this test comes from the inability of the column drain control to handle hits in two consecutive bunch crossings. This leads to the loss of a calibration signal when a beam particle happens to hit the same double-column in the bunch-crossing before the test signal is injected. The probability for this to happen can be measured by counting hits in a double column for randomly triggered events which is also shown in fig.1. Other losses, such as time-stamp buffer overflow contribute as well as the beam intensity increases.

Using the scintillator trigger, the efficiency for beam particles can also be measured. An effi-

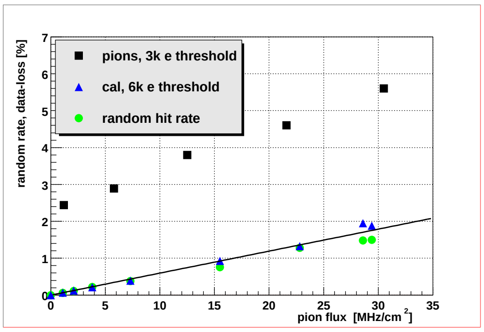

Figure 1. Data-loss measured with calibration signals and beam particles. The data-loss for calibration signals is almost equal to the random hit rate per double column, which is expected when the CD-setup is the dominant source of dead-time. The straight line shows the expected hit rate based on intensity and double-column area.

ciency of 98% for very low intensity is found, dropping to about 95% for the particle flux expected in the innermost detector layer at full LHC luminosity.

Offset and slope of the inefficiency are higher than expected. Similar slopes for calibration signals have been observed for very low settings of the comparator threshold. The reason for this behavior is not clear but it may indicate unwanted induced activity for low comparator thresholds in the region of 3000 electrons.

3. Barrel module construction

All three layers of the pixel barrel will made with the same module design (2). Each module holds 16 readout chips bump-bonded to a sensor using a procedure developed in-house at PSI. Mechanical stability is provided by a silicon baseplate onto which the chips with sensor are glued. The chips periphery with wire-bond pads extends beyond the sensor and is connected with wire-bonds to a high density interconnect (HDI) glued to the back-side of the sensor. The HDI is a three metal layer design with 6 μm trace thickness and 7 μm polyimid layers. To avoid long bond-wires the HDI bends down from the sensor to the chips where it is fixed near the bond-pads. All components have been fabricated and first modules were built to develop the assembly procedure. The modules have a weight of 4 grams including the cables.

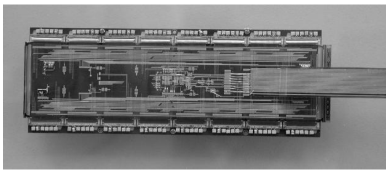

Figure 2. Barrel module. A module has one sensor with 16 readout chips in two rows. A high density interconnect glued onto the back-side of the sensor distributes poser and signals.

4. Readout chip translation

It has become clear over the last years that radiation hard chips can not only be made with radiation hardened processes like DMILL but also with commercially available deep-submicron CMOS technologies when radiation tolerant layout rules are used [5]. The next iteration of the CMS pixel readout chip was developed in a 0.25 μm technology. The design follows closely the PSI43 architecture. The much higher device density available in 0.25 μm technologies permits to remove some of the limitations built into the DMILL design.

The column drain mechanism is now able to process hits in consecutive bunch crossings and can now buffer 3 column drain requests. The size of the time-stamp buffer was increased from 9 to 12 time-stamps and the data-buffers from 24 to 32 hits. With these changes the readout chip can be used in the 4 cm layer at high luminosity with less than 1% data-loss. This was not originally foreseen for the DMILL design. The size reduction of the periphery from 2.8 mm to 1.8 mm is beneficial for module and barrel construction. The size of

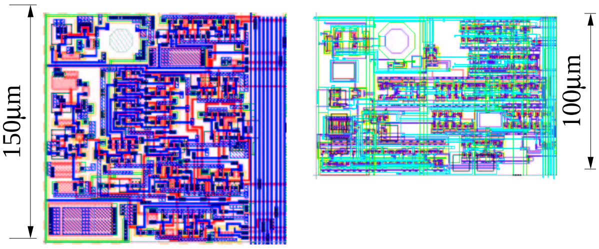

Figure 3. Layout of a pixel cell in the DMILL chip (left) and the 0.25μm chip(right). The designs are similar with some new functionality. The device count went from 127 to 251, the length was reduced to 100 μm

pixel cell itself was reduced to 100 μm × 150 μm although the number of transistors per pixel approximately doubled. The size reduction is in the direction of the Lorentz-drift and improves charge sharing after irradiation. The design was submitted for fabrication in July 2003.

5. Conclusions

A major milestone for the development of the CMS pixel detector has been achieved with the fabrication of the first full readout chip designed in DMILL technology. This chip has been operated successfully in a high rate test beam at PSI with a charged particle flux comparable to LHC conditions. Data-losses in the readout architecture were found in agreement with simulations but the overall inefficiency for beam particles was below expectations. First barrel modules with with PSI43 chips have been assembled for evaluation. A new readout chip in 0.25 μm technology has been designed and submitted for fabrication. It is based on the PSI43 design but will remove its most severe limitations and should be adequate for the highest data rates encountered in the CMS pixel detector.

REFERENCES

1. The CMS collaboration, *CMS Tracker Technical Design Report*, CERN/LHCC 98-6.
2. R. Baur, R. Horisberger, R. Schnyder, M. Lechner, B. Meier, in *Proceedings of the Fourth Workshop on Electronics for the LHC*, CERN/LHCC 98-36.
   R. Baur [CMS Pixel Collaboration], Nucl. Instrum. Meth. A **465**, 159 (2000).
3. M. Dentan *et al.*, IEEE Trans. Nucl. Sci. **43** (1996), p. 1763.
4. D. Kotlinski, Nucl. Instrum. Meth. A **477**, 446 (2002).
5. Nucl. Instrum. Meth. A **439**, 349 (2000).